

FIG. 1

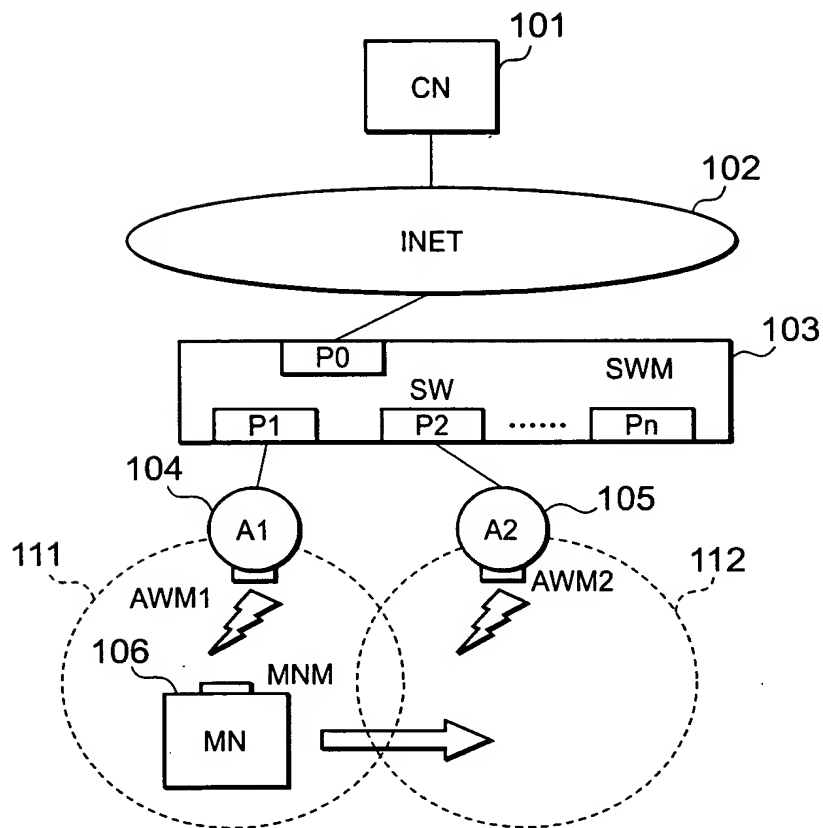


FIG. 2

MAC ADDRESS	OUTPUT PORT
AWM1	P1
AWM2	P2

FIG. 3

MAC ADDRESS	OUTPUT PORT
MNM	P1

FIG. 4A

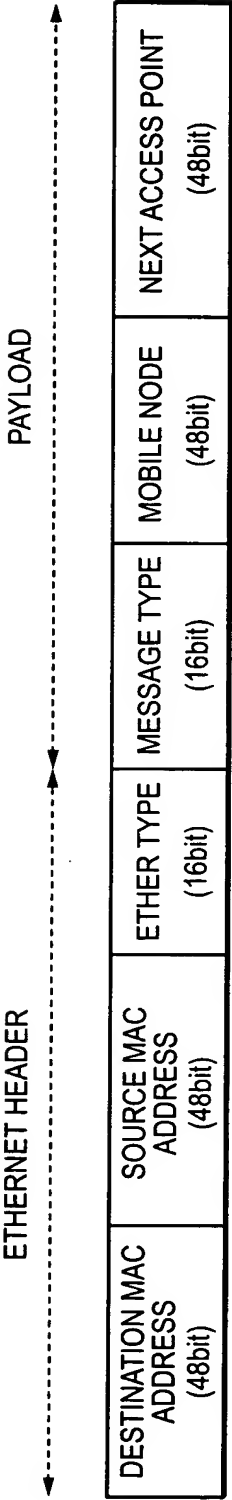


FIG. 4B

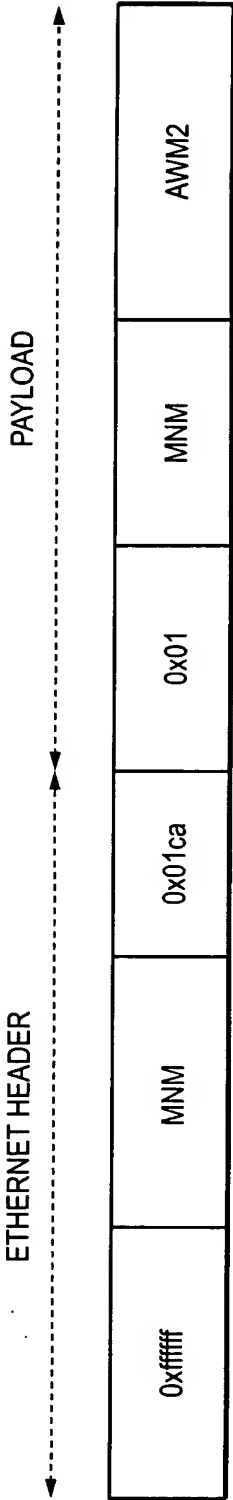


FIG. 5

MAC ADDRESS	OUTPUT PORT
MNM	P2

FIG. 6

MAC ADDRESS	OUTPUT PORT
MNM	P1
MNM	P2

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FIG. 7A

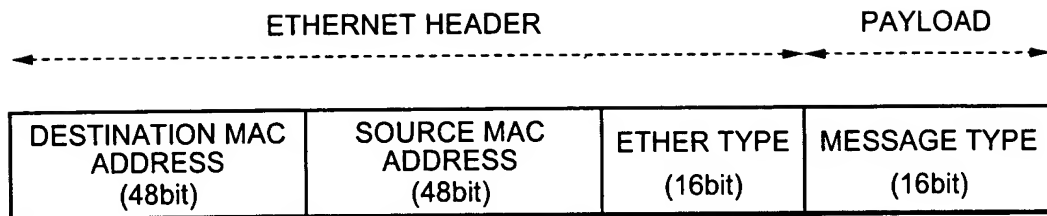


FIG. 7B

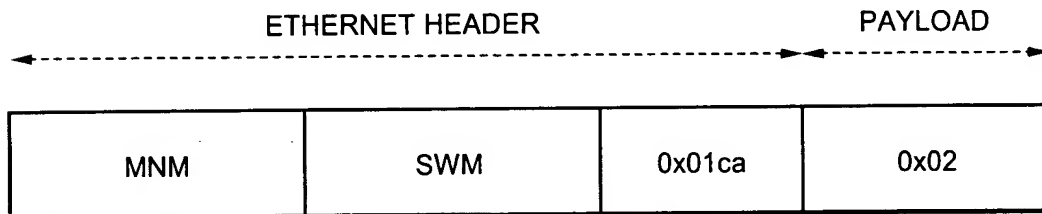


FIG. 8A

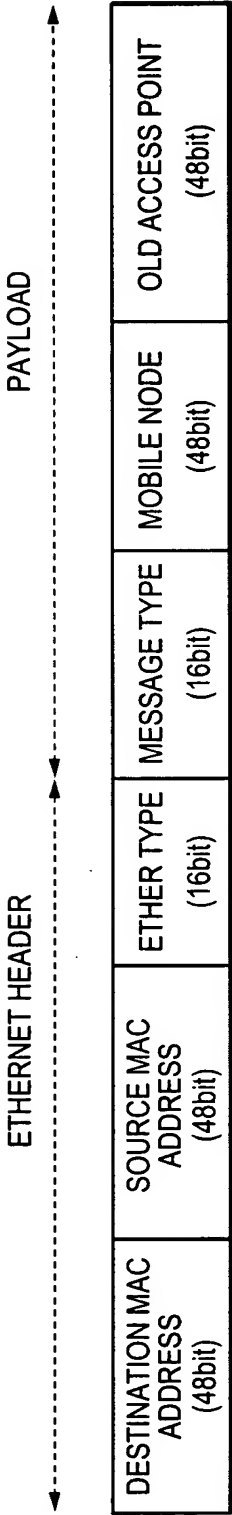


FIG. 8B

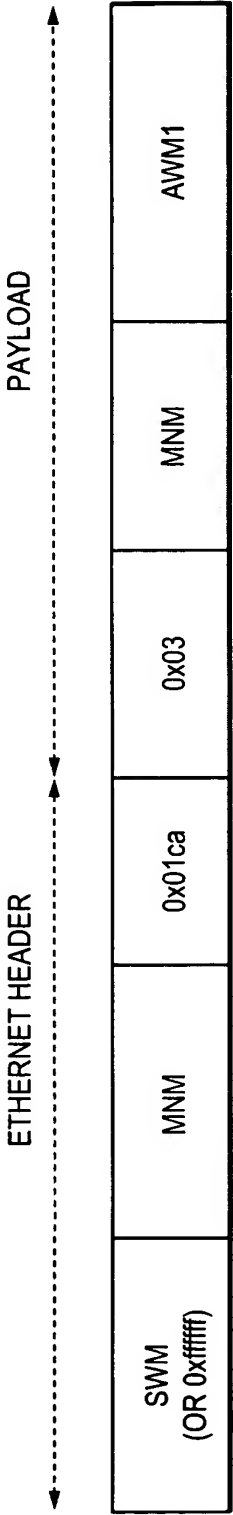


FIG. 9A

MAC ADDRESS	OUTPUT PORT
00:01:02:83:04:86	1

FIG. 9B

MAC ADDRESS	OUTPUT PORT
00:01:02:83:04:86	1
00:01:02:83:04:86	2

FIG. 9C

MAC ADDRESS	OUTPUT PORT
00:01:02:83:04:86	2

FIG. 10

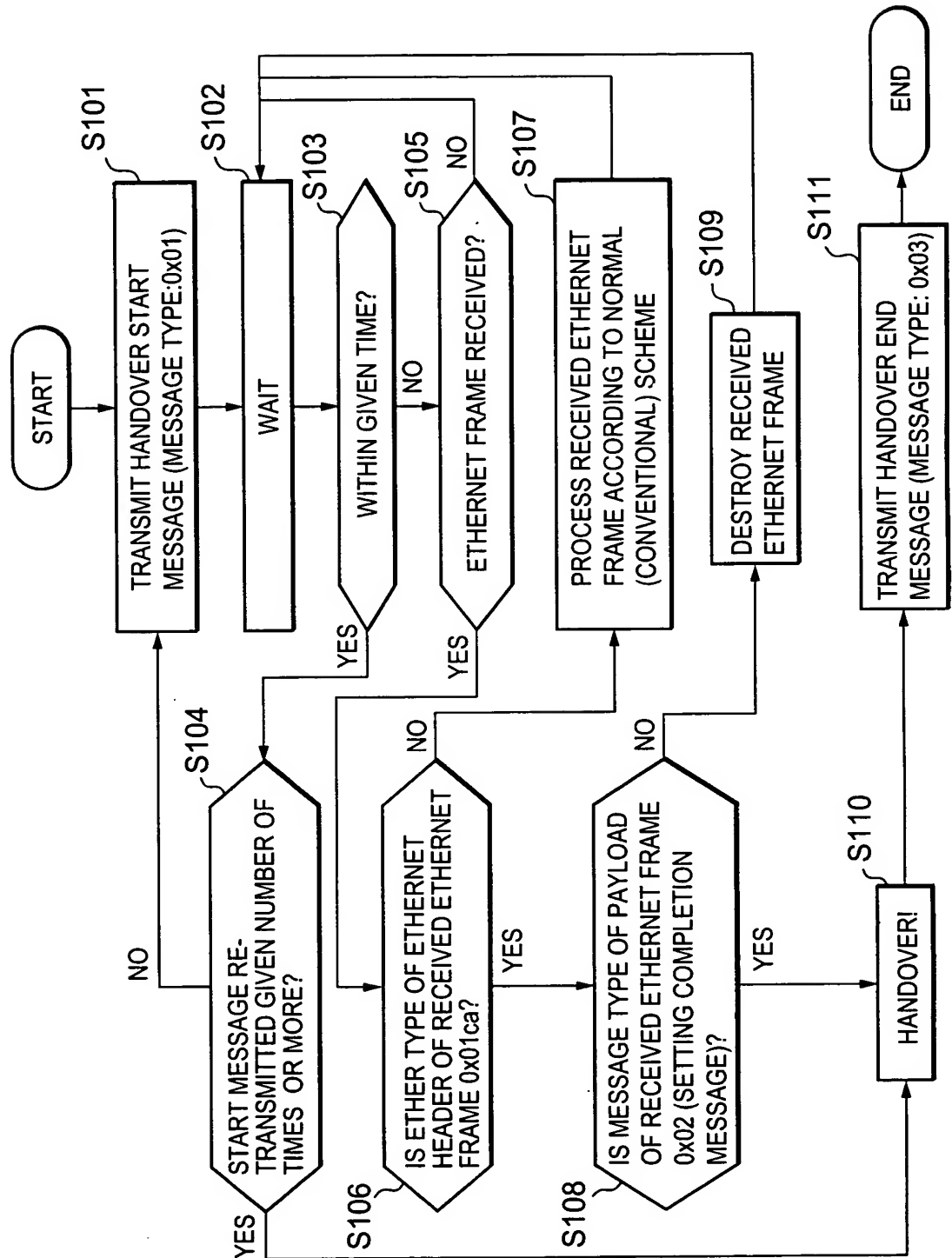


FIG. 11

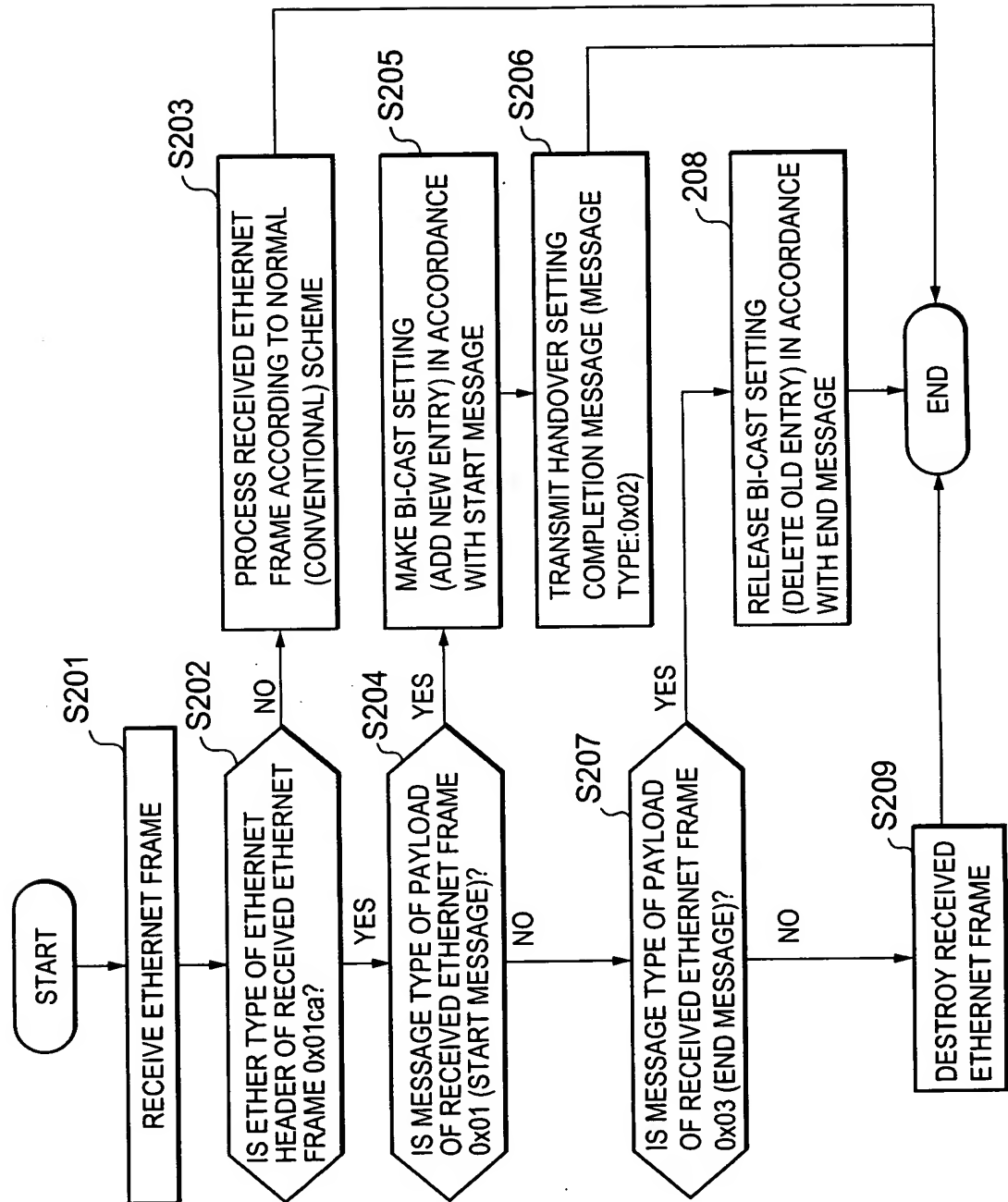


FIG. 12

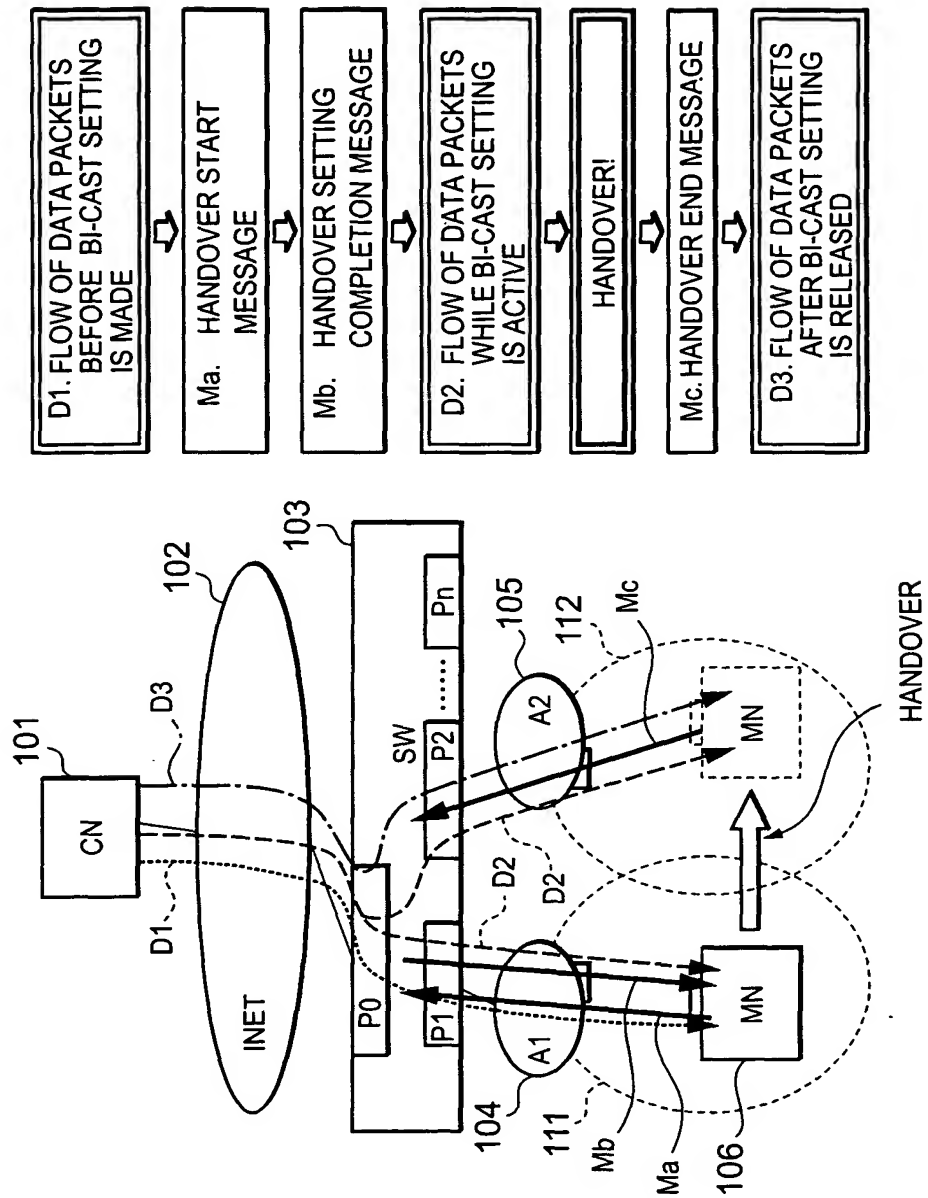


FIG.13

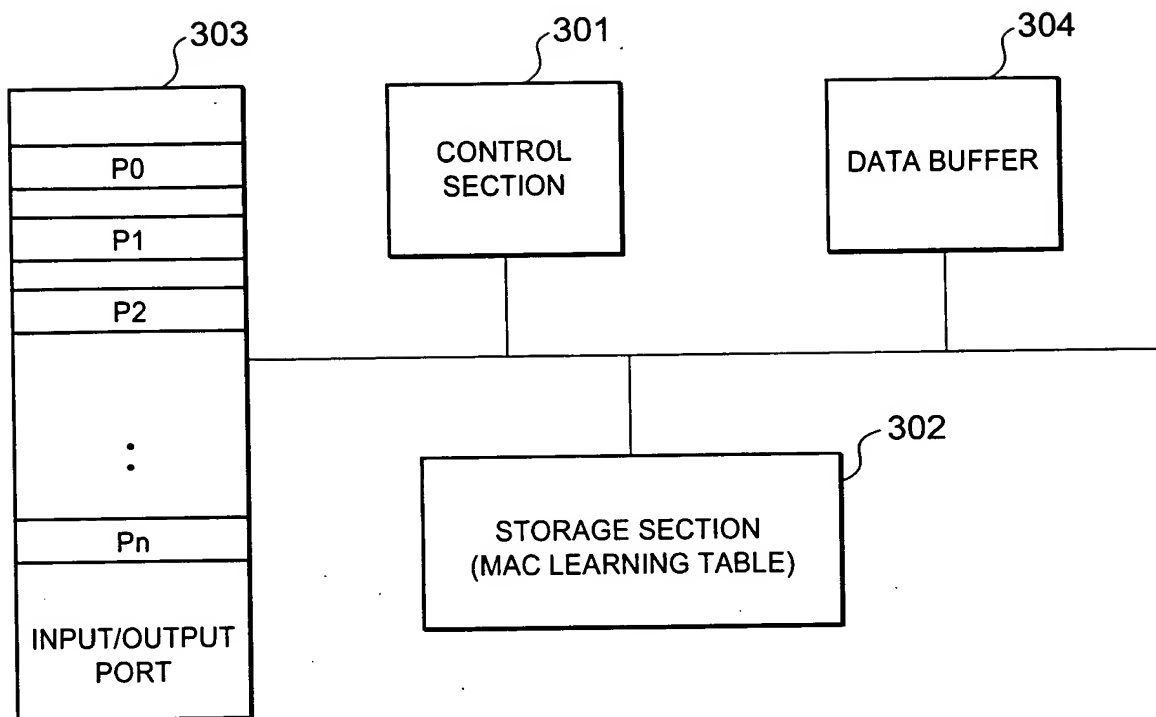


FIG. 14

